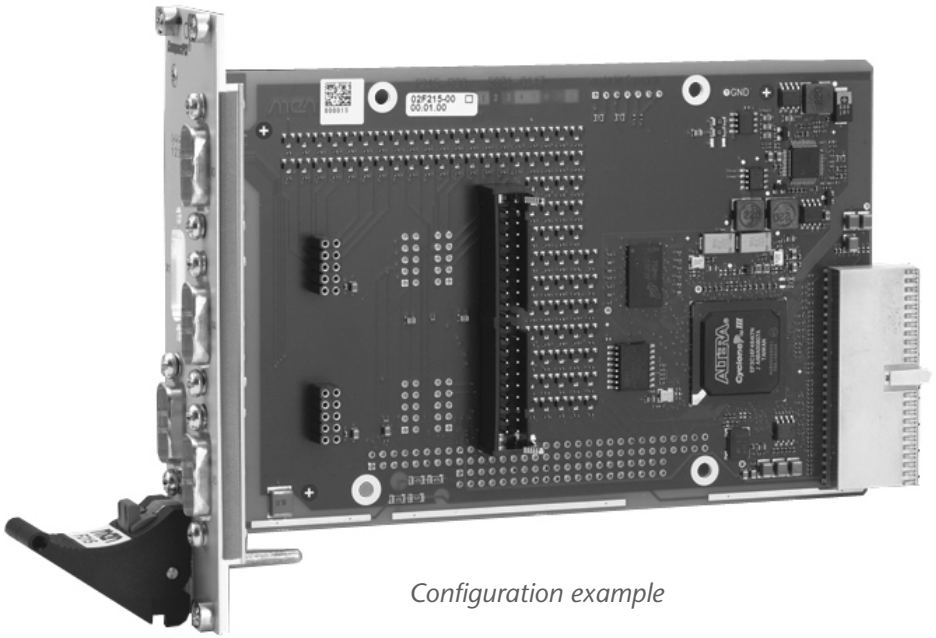
Embedded Solutions

F215 – 3U CompactPCI®
Universal Interface Board



Configuration example

User Manual

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F215 – 3U CompactPCI® Universal Interface Board

The F215 is a universal interface board based on 3U CompactPCI®. The physical layer can be realized individually for each channel by means of SA-Adapters™.

SA-Adapters™ are small universal boards providing the line drivers for legacy serial I/O, fieldbus interfaces and other small I/O functions. Most SA-Adapters™ use 9-pin D-Sub connectors which are accessible at the front panel. Alternatively, the adapter can be connected to the front panel via ribbon cable. The SA concept allows to add additional I/O interfaces to the F215, enhancing flexibility with regard to the line transceivers and isolation requirements.

Two SA-Adapters™ can be mounted directly on the F215, the other maximum six adapters need more front-panel space and are connected to the carrier via ribbon cable. The F215 comes in a standard configuration with five pre-defined functions on 8 HP: two CAN interfaces, two UARTs and one 8-channel binary I/O interface. SA-Adapters™ are not included in the delivery, because different types are available, e.g. for the UARTs. They can be ordered as needed.

The board's I/O functions are realized by means of an FPGA, making it a very flexible, inexpensive solution for dedicated serial I/O. The card can become "everything" from a customized I/O combination to a specialized 8-port CAN card or even an intelligent I/O board including a Nios® soft core, on 4, 8 or 12 HP. The FPGA is loaded automatically after power-up from a 4 MB serial Flash. It is also possible to access this Flash from the CompactPCI® bus to update its contents.

The F215 is designed for use in rugged environments. For example, all components are soldered-on and are specified for an operating temperature of -40 to +85°C.

Technical Data

I/O Interfaces

- Different variations possible through FPGA IP cores and SA-Adapters™:
  - RS232
  - RS422
  - RS485
  - IBIS master/slave
  - CAN bus
  - HDLC
  - Binary I/O
  - The FPGA offers the possibility to add customized I/O functionality. See FPGA.
  - Option matrix showing possible IP cores and SA-Adapters™ (PDF)
- Accessible via onboard connectors
  - Physical interface at front panel using SA-Adapters™
  - Two interfaces for direct onboard connection of SA-Adapters™
  - Up to six interfaces for connection of SA-Adapters™ via 10-pin ribbon cable
- Standard factory interface configuration:
  - 8 HP front panel with five SA-Adapter™ cut-outs for
  - 2 CAN bus interfaces
  - 2 UART interfaces
  - 1 binary I/O interface
  - No SA-Adapters™ included by standard; they can be selected as needed
- Standard factory FPGA configuration:
  - 16Z029_CAN – CAN controller (controls CAN X1)
  - 16Z029_CAN – CAN controller (controls CAN X2)
  - 16Z125_UART – UART controller (controls UARTs X3/X4)
  - 16Z037_GPIO – GPIO controller (8 I/O lines on X5)

Memory

- 4 MB serial Flash for FPGA configuration

Miscellaneous

- Four status LEDs at front panel
  - One status LED to signal FPGA configuration (interfaces ready)
  - Three user LEDs, FPGA-controlled by 16Z034_GPIO controller

Local PCI Bus

- 32-bit/33-MHz, 3.3 V V(I/O)
- Compliant with PCI Specification 2.2

CompactPCI® Bus

- Compliance with CompactPCI® Core Specification PICMG 2.0 R3.0
- Peripheral slot
- V(I/O): +3.3 V

Electrical Specifications

- Supply voltage/power consumption:
  - +5 V (-3%/+5%), current depends on mounted SA-Adapters™; 200 mA without SA-Adapters™
  - +3.3 V (-3%/+5%), 150 mA typ.

Mechanical Specifications

- Dimensions: conforming to CompactPCI® specification for 3U boards
- Front panel: 8 HP with ejector
  - For up to five interfaces
- Weight: 175 g (w/o SA-Adapters™)

Environmental Specifications

- Temperature range (operation):
  - -40..+85°C (qualified components)
  - Airflow: min. 1.0 m/s
- Temperature range (storage): -40..+85°C
- Relative humidity (operation): max. 95% non-condensing
- Relative humidity (storage): max. 95% non-condensing
- Altitude: -300 m to +3000 m
- Shock:
  - 15 g, 11 ms (EN 60068-2-27)
  - 50 m/s², 30 ms (EN 61373)
- Bump: 10 g, 16 ms (EN 60068-2-29)
- Vibration (sinusoidal): 1 g, 10 Hz – 150 Hz (EN 60068-2-6)
- Vibration (function): 1 m/s², 5 Hz – 150 Hz (EN 61373)
- Vibration (lifetime): 7.9 m/s², 5 Hz – 150 Hz (EN 61373)
- Conformal coating on request

MTBF

- 383 944 h @ 40°C according to IEC/TR 62380 (RDF 2000)

Safety

- PCB manufactured with a flammability rating of 94V-0 by UL recognized manufacturers

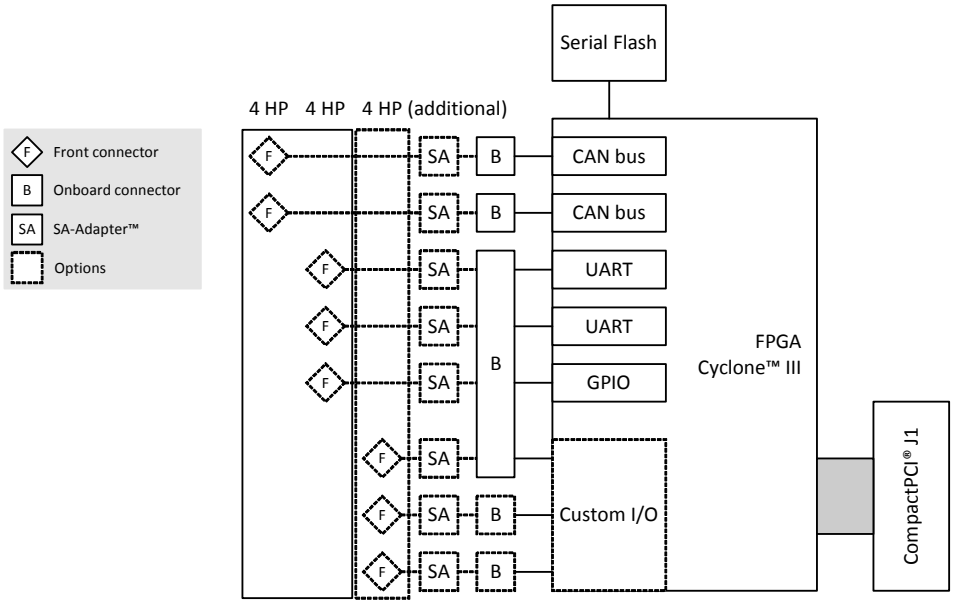
EMC

- Tested according to EN 55022 (radio disturbance), IEC 61000-4-2 (ESD) and IEC 61000-4-4 (burst)

Software Support

- Driver software for Windows®, Linux, VxWorks®, QNX®
- Flash update tools for Windows®, Linux, VxWorks®
- For more information on supported operating system versions and drivers see online data sheet.

Block Diagram



Configuration Options

Physical Layers

- Via up to eight SA-Adapters™
- Different variations possible through FPGA IP cores and SA-Adapters™:
  - RS232
  - RS422
  - RS485
  - IBIS master/slave
  - CAN bus
  - HDLC
  - Binary I/O
  - InterBus-S
  - GPS
  - Other physical layers dependent on FPGA configuration
  - Option matrix showing possible IP cores and SA-Adapters™ (PDF)

Mechanical

- 4, 8 or 12 HP front panel dependent on number of SA-Adapters™
  - 4 HP with 2 onboard SA-Adapters™
  - 8 HP with 5 SA-Adapters™ (standard)
  - 12 HP with 8 SA-Adapters™
- One-piece front panel

Cooling Concept

- Also available with conduction cooling in MEN CCA frame

Please note that some of these options may only be available for large volumes. Please ask our sales staff for more information.

For available standard configurations see online data sheet.

FPGA

This product offers the possibility to add customized I/O functionality in FPGA.

Flexible Configuration

- Customized I/O functions can be added to the FPGA.
- It depends on the board type, pin counts and number of logic elements which IP cores make sense and/or can be implemented. Please contact MEN for information on feasibility.
- You can find more information on our web page "User I/O in FPGA"

FPGA Capabilities

- FPGA Altera® Cyclone® III EP3C40
  - 39 600 logic elements
  - 1134 Kbits total RAM
- For interface functions
- 4 MB external Flash for FPGA configurations
- Connection
  - Total available pin count: 64 pins
  - Functions available via onboard I/O connectors
  - SA-Adapters™ are used to realize the physical lines.
- Functional updates via software
  - MEN offers Flash update tools for different operating systems.
- Option matrix showing possible IP cores and SA-Adapters™ (PDF)

Product Safety

Electrostatic Discharge (ESD)

Computer boards and components contain electrostatic sensitive devices. Electrostatic discharge (ESD) can damage components. To protect the board and other components against damage from static electricity, you should follow some precautions whenever you work on your computer.

- Power down and unplug your computer system when working on the inside.
- Hold components by the edges and try not to touch the IC chips, leads, or circuitry.
- Use a grounded wrist strap before handling computer components.
- Place components on a grounded antistatic pad or on the bag that came with the component whenever the components are separated from the system.
- Store the board only in its original ESD-protected packaging. Retain the original packaging in case you need to return the board to MEN for repair.

About this Document

This user manual is intended only for system developers and integrators, it is not intended for end users.

It describes the hardware functions of the board, connection of peripheral devices and integration into a system. It also provides additional information for special applications and configurations of the board.

The manual does not include detailed information on individual components (data sheets etc.). A list of literature is given in the appendix.

History

Issue	Comments	Date
E1	First issue	2008-11-17
E2	General update, minor errors corrected; additions and clarifications in functional description	2009-03-20
E3	Added chapters 2.3.2.3 to 2.3.2.6, corrected table 9	2010-12-13
E4	Complete review of manual, especially links, drawings and description of driver software	2012-02-15
E5	Removed DDR2 RAM (no longer assembled)	2012-11-05

Conventions

This sign marks important notes or warnings concerning the use of voltages which can lead to serious damage to your health and also cause damage or destruction of the component.

This sign marks important notes or warnings concerning proper functionality of the product described in this document. You should read them in any case.

italics — Folder, file and function names are printed in *italics*.

bold — **Bold** type is used for emphasis.

`monospace` — A `monospaced` font type is used for hexadecimal numbers, listings, C function descriptions or wherever appropriate. Hexadecimal numbers are preceded by "0x".

comment — Comments embedded into coding examples are shown in green color.

hyperlink — Hyperlinks are printed in blue color.

The globe will show you where hyperlinks lead directly to the Internet, so you can look for the latest information online.

IRQ# /IRQ — Signal names followed by "#" or preceded by a slash ("/") indicate that this signal is either active low or that it becomes active at a falling edge.

in/out — Signal directions in signal mnemonics tables generally refer to the corresponding board or component, "in" meaning "to the board or component", "out" meaning "coming from it".

Vertical lines on the outer margin signal technical changes to the previous issue of the document.

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Since July 1, 2006 all MEN standard products comply with RoHS legislation.

Since January 2005 the SMD and manual soldering processes at MEN have already been completely lead-free. Between June 2004 and June 30, 2006 MEN's selected component suppliers have changed delivery to RoHS-compliant parts. During this period any change and status was traceable through the MEN ERP system and the boards gradually became RoHS-compliant.

WEEE Application

The WEEE directive does not apply to fixed industrial plants and tools. The compliance is the responsibility of the company which puts the product on the market, as defined in the directive; components and sub-assemblies are not subject to product compliance.

In other words: Since MEN does not deliver ready-made products to end users, the WEEE directive is not applicable for MEN. Users are nevertheless recommended to properly recycle all electronic boards which have passed their life cycle.

Nevertheless, MEN is registered as a manufacturer in Germany. The registration number can be provided on request.

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1 Getting Started

This chapter gives an overview of the board and hints for first installation in a system.

1.1 General Concept

The F215 is a universal interface board with a maximum of 8 interfaces. All of the board's I/O functions are realized inside its FPGA, making it a very flexible solution for dedicated serial I/O. The physical layer is implemented individually for each channel by means of MEN standard SA-Adapters.

Two SA-Adapters can be mounted directly on the F215, the other maximum six adapters need more front-panel space and are connected via ribbon cable.

The standard version of F215 lets you connect up to five SA-Adapters to implement its line interfaces on 8 HP (two slots). Two SA-Adapters for CAN bus can be mounted directly on the board (see Chapter 1.4.1 Direct Connection (X1, X2) on page 18), the other three adapters (two UARTs, one binary I/O interface) are connected via ribbon cable and led to the second front-panel slot (see Chapter 1.4.2 Connection via Ribbon Cable (X3, X4, X5) on page 20).

Suitable SA-Adapters are available for all interface types of the standard version, with different options for the UARTs, e.g., RS232, RS422/485 or IBIS master/slave.

With two additional connectors assembled, the F215 supports up to eight different interfaces.

For ordering information of available SA-Adapters please see the F215 data sheet on MEN's website.

Ask our sales team for tailor-made, custom assembly and configuration options.

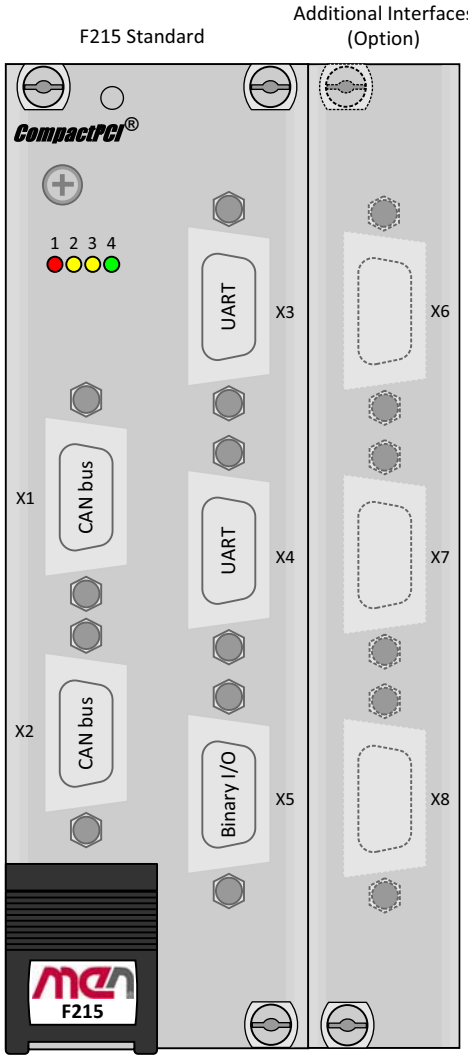
For details on...

- CAN bus functions see Chapter 2.3.1 CAN Bus Interfaces on page 25.
- UART functions see Chapter 2.3.2 UART Interfaces on page 26.
- binary I/O functions see Chapter 2.3.3 Binary I/O Interface on page 32.
- front-panel LEDs see Chapter 2.4 Front-Panel LEDs on page 34.
- FPGA see Chapter 3 FPGA on page 35.

1.2 Front Panel and Interfaces

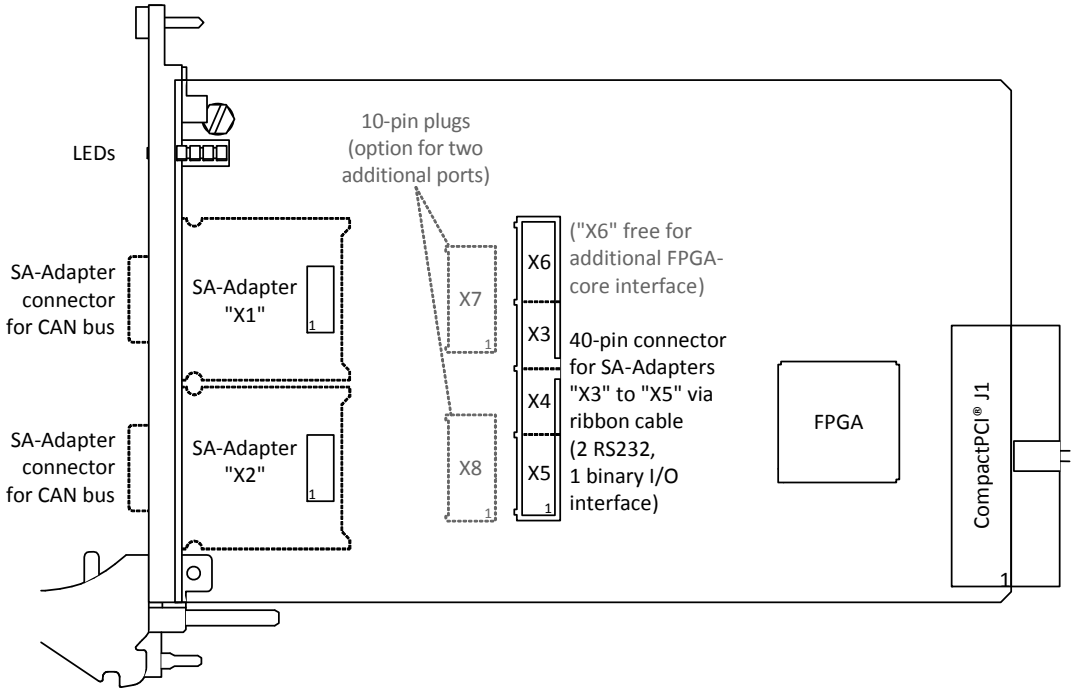
The F215 has five slots for standard 9-pin D-Sub connectors at the front. The standard configuration includes two CAN-bus interfaces, two UARTs and one 8-bit binary I/O port.

Figure 1. *Front panel and interfaces*



1.3 Map of the Board

Figure 2. *Map of the board (top view)*



1.4 Installing SA-Adapters

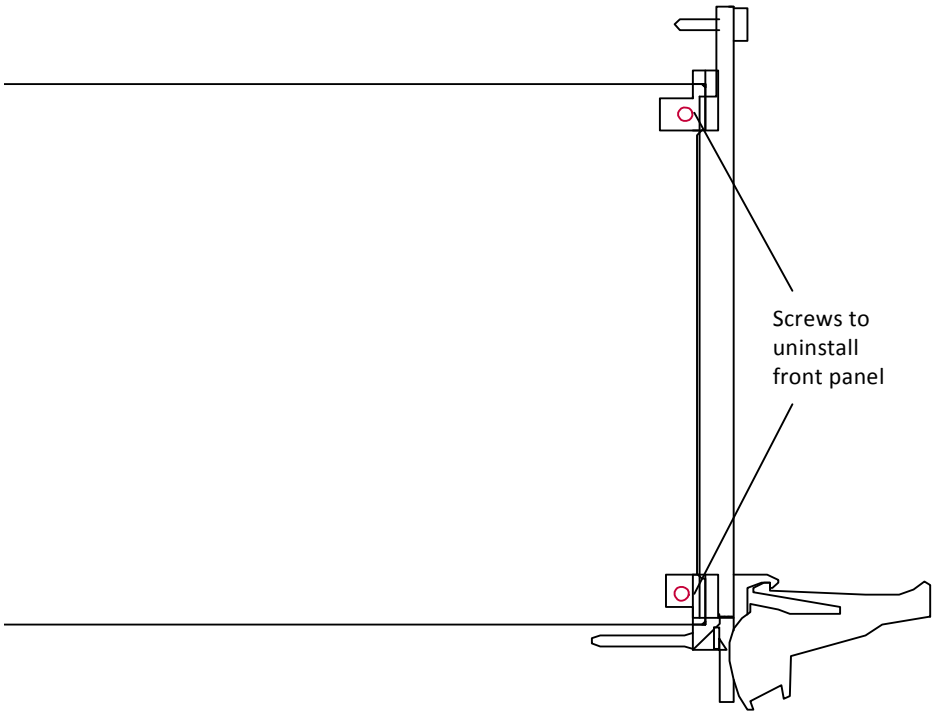
1.4.1 Direct Connection (X1, X2)

Two SA-Adapters can be mounted directly on the F215 on the 10-pin receptacle connectors "X1" and "X2".

☑ Make sure that the adapter matches the standard dimensions for SA-Adapters. (See also installation hints in the adapter's user manual or the list of compatible accessories in the F215 data sheet on MEN's website.)

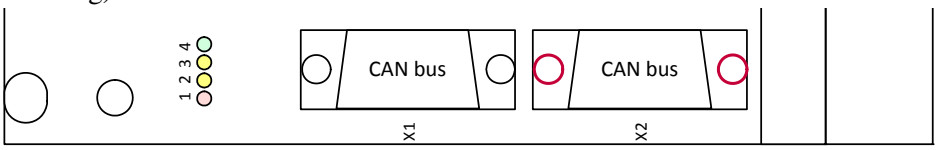
☑ Power down your system and remove the F215 from the system.

☑ Remove the front panel: Loosen and remove the two screws highlighted in red.



☑ Remove the two front panel screws and the two screws on top of the mounting bolts of the SA-Adapter.

☑ Remove the blind connector from the front panel, if you need a slot that is covered: Loosen the two screws at the front of the panel (highlighted in red in the drawing).



Hint: Hold the screw in place with a suitable tool from the back of the panel, then loosen the screw at the front.

☑ The SA-Adapter is plugged on the F215 with the component sides of the PCBs facing each other.

☑ Carefully put it down, making sure that the connectors are properly aligned.

☑ Press the SA-Adapter firmly onto the F215.

☑ Reinstall the front panel: Place the front panel back over the connectors, taking care not to damage the LEDs.

☑ Put back and fasten the two front-panel screws removed before.

☑ Screw the SA-Adapter tightly to the F215 PCB using the two pan-head screws removed before.

Figure 3. *Installing SA-Adapters on F215 directly*

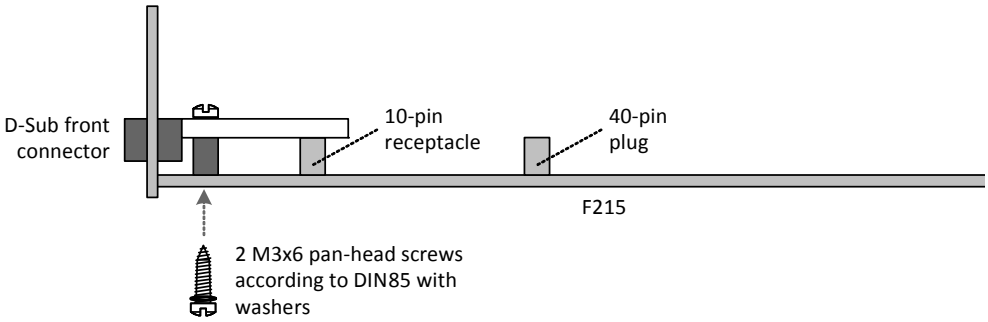
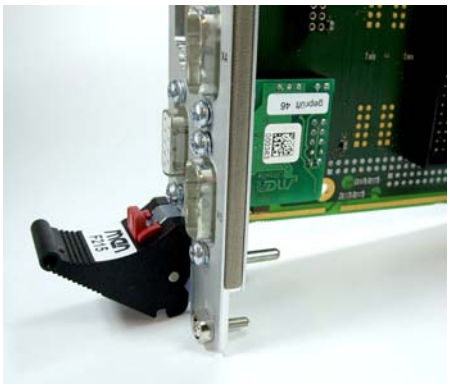


Figure 4. *F215 with one CAN-bus SA-Adapter on X1*



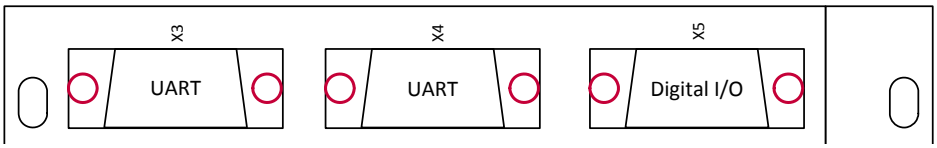
1.4.2 Connection via Ribbon Cable (X3, X4, X5)

A suitable 40-pin connector with ribbon cables leading to three 10-pin SA-Adapter receptacles is included in the delivery of the F215. This allows easy installation of SA-Adapters in slots "X3", "X4" and "X5".

Note: MEN gives no warranty on functionality and reliability of the board and SA-Adapters used if you install SA-Adapters in a different way than described in MEN's documentation.

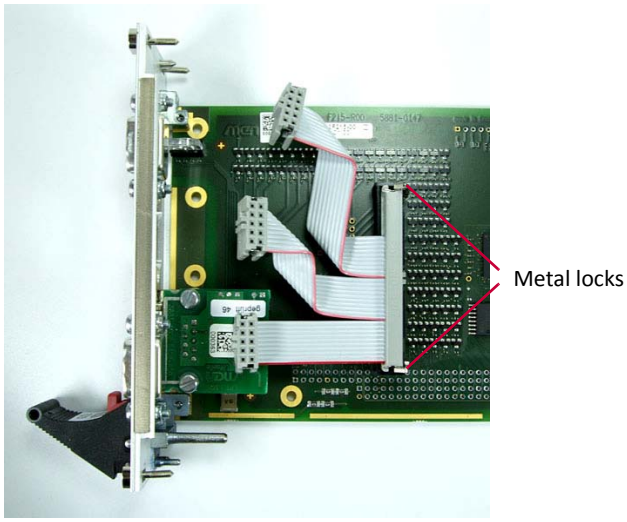
Perform the following steps to install SA-Adapters in X3, X4 or X5:

- ☑ Make sure that the adapter matches the standard dimensions for SA-Adapters. (See also installation hints in the adapter's user manual or the list of compatible accessories in the F215 data sheet on MEN's website.)
- ☑ Power-down your system and remove the F215 from the system.
- ☑ Remove the blind connector from the additional front panel: Loosen one of the screw pairs highlighted in the drawing.



- ☑ Remove the two front panel screws and the two screws on top of the mounting bolts of the SA-Adapter.

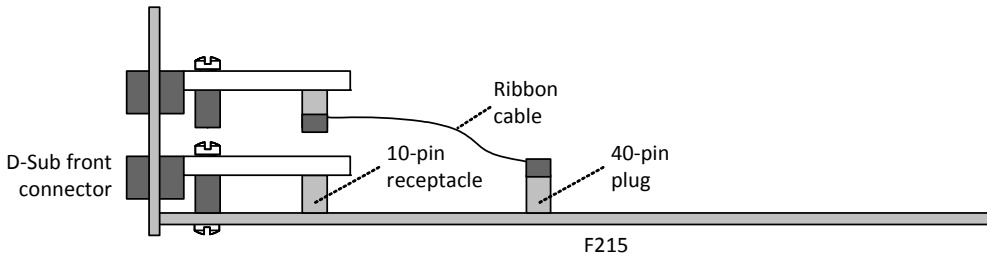
☑ Plug the 40-pin connector with the three prefolded ribbon cables to the 40-pin plug of the carrier board and close the metal locks.



☑ Plug the suitable 10-pin connector of the ribbon cable to the respective 10-pin SA-Adapter connector.
Make sure to always align the pins correctly (pin 1 is marked by a triangle on the ribbon cable connector).

☑ Use the front panel screws of the SA-Adapters to fasten the adapters at the additional front panel.

Figure 5. *Installing SA-Adapters via ribbon cable in slots X3, X4 and X5*



☑ You can now reinsert the board and the additional front panel into your system. Make sure to fasten the SA-Adapter front panel appropriately in your enclosure!

Figure 6. *F215 with one CAN-bus SA-Adapter on X2 and one RS232 SA-Adapter on X4*

1.5 Integrating the Board into a System

You can use the following check list when installing the board in a system for the first time.

- ☑ Install the desired SA-Adapters on the F215. (See Chapter 1.4 Installing SA-Adapters on page 18.)
- ☑ Power-down the system.
- ☑ Insert the F215 into a peripheral slot of your CompactPCI system, making sure that the CompactPCI connectors are properly aligned.

  Note: The peripheral slots of every CompactPCI system are marked by a circle ○ on the backplane and/or at the front panel.
- ☑ Power-up the system.
- ☑ You can now install driver software for the F215 I/O interfaces.

1.6 Installing Driver Software

For a detailed description on how to install driver software please refer to the respective documentation.

You can find any driver software available for download on MEN's website.

2 Functional Description

2.1 Power Supply

Power supply is fed via the CompactPCI backplane. The board operates on +3.3 V and +5 V.

2.2 Board Configuration

The F215 has a fixed standard configuration for you to get started. However, the board is completely open for a final configuration that 100% suits your application.

In addition to the possible hardware configuration and assembly options explained in Chapter 1.1 General Concept on page 15, the F215 also allows to include more advanced features. The basis of its flexibility is the F215's Altera Cyclone III FPGA with 39,600 logic elements, 1,134 Kbits total RAM and 4 MB configuration Flash. See also Chapter 3 FPGA on page 35.

In any case we recommend that you contact our sales team for tailor-made, custom assemblies. This chapter only summarizes the board's options.

2.2.1 I/O Interfaces

The onboard FPGA permits many possible combinations of different standard IP cores for a total of eight interfaces. The assignment of connectors to the individual functions is just as flexible. (See also Chapter 4.1 Assignment of Onboard Connectors to Front-Panel Slots on page 37.)

On its website MEN provides an option matrix that includes possible functions along with software support for the different operating systems and SA-Adapters that can be used as physical layers.

You can also find an overview of configuration options in the F215 data sheet, also on MEN's website.

2.2.2 Nios Soft Processor

The F215 can become more than a pure I/O board when inexpensive intelligence is added through a Nios soft core. A typical type would be the Nios II/f processor. It could be utilized, for instance, to pre-process data.

A suitable design environment is available from Altera.

2.3 Standard Interfaces

2.3.1 CAN Bus Interfaces

The F215 offers two CAN interfaces on two 10-pin receptacle connectors for direct connection of MEN SA-Adapters, which have standard 9-pin D-Sub connectors.

The CAN controller is a standard IP core from MEN called 16Z029_CAN. MEN offers a standard adapter for CAN bus, the SA8.

The interfaces support the 2.0 A/B CAN protocol. Typical CAN-bus bit rates are:

- 1 Mbit/s (maximum)
- 800 kbit/s
- 500 kbit/s
- 250 kbit/s
- 125 kbit/s
- 100 kbit/s
- 50 kbit/s (minimum)

Please see MEN's website for ordering information of SA-Adapters.

You can find more information in the 16Z029_CAN data sheet on MEN's website.

Please see MEN's website for up-to-date driver software and documentation.

See also Chapter 4.3 Literature and Web Resources on page 38 for literature on CAN bus.

2.3.1.1 Connection

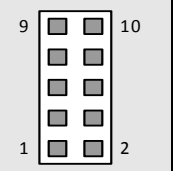
Connector types:

- 10-pin receptacle, 2.54 mm pitch, for SA-Adapter connection

Mating connector:

- 10-pin SA-Adapter plug

Table 1. *Pin assignment of the 10-pin CAN bus receptacle connectors (X1/X2)*



9	-	10	-
7	-	8	-
5	-	6	-
3	CAN_TX	4	CAN_RX
1	GND	2	VCC

Table 2. *Signal mnemonics of CAN bus interfaces (X1/X2)*

Signal	Direction	Function
CAN_RX	in	CAN bus data receive line
CAN_TX	out	CAN bus data transmit line
GND	-	Reference potential
VCC	out	Power supply

2.3.2 UART Interfaces

The F215 offers two standard UARTs that can be configured as a non-differential (single-ended) RS232, or differential RS422 (full duplex) or RS485 (half duplex) interface with full handshake support. The physical layers are defined through SA-Adapters, and can be set individually for each channel through software. (See software documentation for more details.)

MEN provides a range of standard adapters with different line interfaces, e.g. RS232, RS422/485, or IBIS.

The UART controller is a standard IP core from MEN called 16Z125_UART.

Please see MEN's website for ordering information of SA-Adapters.

You can find more information in the 16Z125_UART data sheet on MEN's website.

Please see MEN's website for up-to-date driver software and documentation.

The register set of the octal UART is fully 16550D compatible. Data rates up to 921 600 bit/s are possible, depending on the physical interface type selected.

2.3.2.1 Connection

All UART ports are available on the F215's 40-pin onboard connector. An adapter connector with ribbon cables is included in the standard delivery to spread the 40-pin connector to three SA-Adapter receptacles. (See Chapter 1.4 Installing SA-Adapters on page 18.)

Note: Some SA-Adapters do not support all signals. Please refer to the user manual of the actually used SA-Adapter for details. See Chapter 4.3 Literature and Web Resources on page 38.

Connector types:

- 40-pin low-profile plug, 2.54 mm pitch, for ribbon-cable connection
- Mating connector:
  40-pin IDC receptacle, e.g. Elco Series 8290 IDC socket

Table 3. *Pin assignment of UARTs (X3/X4) on the 40-pin connector for RS232*

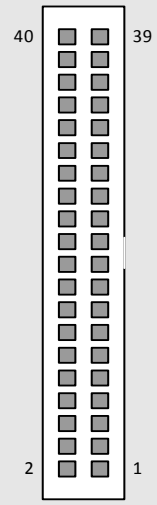
	40 .. 32		39 .. 31		Not used
	30	RI10#	29	DCD10#	X3 UART
	28	CTS10#	27	DSR10#	
	26	RTS10#	25	DTR10#	
	24	RXD10	23	TXD10	
	22	+5V	21	GND	
	20	RI11#	19	DCD11#	X4 UART
	18	CTS11#	17	DSR11#	
	16	RTS11#	11	DTR11#	
	14	RXD11	13	TXD11	
	12	+5V	11	GND	
	10 .. 2		9 .. 1		X5 binary I/O

Table 4. *Pin assignment of UARTs (X3/X4) on the 40-pin connector for RS422*

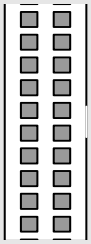
	30	RX10-	29	-	X3 UART
	28	TX10-	27	-	
	26	-	25	RX10+	
	24	-	23	TX10+	
	22	+5V	21	GND	
	20	RX11-	19	-	X4 UART
	18	TX11-	17	-	
	16	-	11	RX11+	
	14	-	13	TX11+	
	12	+5V	11	GND	

Table 5. *Pin assignment of UARTs (X3/X4) on the 40-pin connector for RS485*

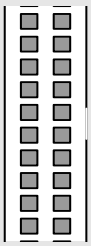
	30	-	29	-	X3 UART
	28	D10-	27	-	
	26	-	25	-	
	24	-	23	D10+	
	22	+5V	21	GND	
	20	-	19	-	X4 UART
	18	D11-	17	-	
	16	-	11	-	
	14	-	13	D11+	
	12	+5V	11	GND	

Table 6. *Signal mnemonics of UART interfaces (X3/X4)*

Mode	Signal	Direction	Function
All modes	GND	-	Ground
	+5V	out	+5V supply voltage
RS422	RX+/-	in	Differential receive data
	TX+/-	out	Differential transmit data
RS485	D+/-	in/out	Differential transceive data
RS232	CTS	in	Clear to send
	DCD	in	Data carrier detected
	DSR	in	Data set ready
	DTR	out	Data terminal ready
	RI	in	Ring indicator
	RTS	out	Request to send
	RXD	in	Receive data
	TXD	out	Transmit data

2.3.2.2 Setting the Physical Layer

The two UART channels can be configured individually as differential RS422 or RS485, or non-differential (single-ended) RS232 interfaces. The setting is made using driver software. For Windows MEN offers a driver installation package that allows easy configuration through the Device Manager. For Linux, VxWorks and QNX MEN also offers driver software that provides the necessary functions to write application software.

The following chapters give hints on how to make settings under the supported operating systems.

For further details on the different driver packages, please refer to the respective software documentation.

Please see MEN's website for up-to-date driver software and documentation.

2.3.2.3 Configuration under Windows

MEN's driver installation package (Installset) for Windows allows easy configuration through the Device Manager.

To do this, open the *Properties* page of each F215 UART device via the Windows Device Manager, select the *Port Interface* tab and choose the used physical interface.

You can find more details on the Windows Installset in the *F215 and G215 Windows Installset User Manual*.

You can download the Windows driver and user manual from MEN's website.

2.3.2.4 Configuration under Linux

MEN provides a Linux driver that allows to configure the interface mode and baud rate.

You can download the Linux driver and documentation from MEN's website.

The *baud_base* parameter must be set to 1843200.

MEN's Linux driver supports the following values for the *mode* parameter:

se	single ended (RS232)
df_fdx	differential, full duplex (RS422)
df_hdxe	differential, half duplex, with echo (RS485)
df_hdx	differential, half duplex, no echo (RS485)

The following examples show how to use the driver with F215.

Set all UART ports to RS232 mode

```
# modprobe men_lx_chameleon usePciIrq=1
# modprobe men_lx_frodo baud_base=1843200 mode=se,se
```

Set all UART ports to RS422 full-duplex mode

In order to change the settings, the driver needs to be removed first.

```
# rmmod men_lx_frodo
# modprobe men_lx_frodo baud_base=1843200 mode=df_fdx,df_fdx
```

Note: Most Linux kernels only support 4 UARTs by default. If you need more than 4 UARTs, add parameter *8250.nr_uarts=48* to your kernel boot line in the bootloader or adjust kernel parameter *CONFIG_NR_8250_UARTS* and recompile the kernel.

2.3.2.5 Configuration under VxWorks

MEN provides a VxWorks driver that provides comprehensive I/O control support to configure the interfaces.

You can find more details on MEN's VxWorks driver software in the driver's included HTML documentation.

You can download the VxWorks driver from MEN's website.

The UART clock frequency must be set to 58982400. You can use driver function *Z25_CreateDevice* or *Z25_SetBaseBaud* to do this.

2.3.2.6 Configuration under QNX

MEN provides a QNX driver that allows configuration of the interfaces through QNX tool *stty*.

The *stty* tool together with MEN's QNX driver provides a large number of parameters to configure serial interfaces. MEN's driver includes options to set the physical interface itself. You can get details on the driver using QNX command *use devc-serz025*.

You can download the QNX driver from MEN's website.

To get details on the driver use QNX command *use devc-serz025*.

You can find more information on *stty* also on the QNX developer community website.

2.3.2.7 Supported Baud Rates

The F215 provides highly accurate baud rates. The following baud rates are supported and tested[1].

Table 7. *Supported and tested baud rates*

Desired Baud Rate [bit/s]	Supported with		
	RS422	RS485	RS232
110	x	x	x
300	x	x	x
1200	x	x	x
2400	x	x	x
4800	x	x	x
9600	x	x	x
19200	x	x	x
38400	x	x	x
57600	x	x	x
115200	x	x	x
230400	x	x	x
460800	x	x	
921600	x	x	

Please note that at higher baudrates the system performance has to be sufficient to process the receive interrupts fast enough to prevent the internal FIFOs from overrunning. It may also be reasonable to reduce the FIFO trigger levels of the F215 UARTs.

[1] Other settings are possible but are not tested.

2.3.3 Binary I/O Interface

The F215 provides 8 I/O ports via a serial SPI interface. The GPIO controller with serial interface is a standard IP core from MEN called 16Z037_GPIO.

MEN's standard binary I/O SA-Adapter, the SA15, de-serializes the SPI data stream and gives access to individual I/O lines at its peripheral connector.

You can control the I/O lines using MDIS5 driver software available from MEN. By default, the GPIOs are configured as inputs. This configuration can be changed through the driver software.

Please see MEN's website for ordering information of SA-Adapters.

You can find more information in the 16Z037_GPIO data sheet on MEN's website.

Please see MEN's website for up-to-date driver software and documentation.

2.3.3.1 Connection

The binary I/O signals are available on the F215's 40-pin onboard connector. An adapter connector with ribbon cables is included in the standard delivery to spread the 40-pin connector to three SA-Adapter receptacles. (See Chapter 1.4 Installing SA-Adapters on page 18.)

Connector types:

- 40-pin low-profile plug, 2.54 mm pitch, for ribbon-cable connection
- Mating connector:
  40-pin IDC receptacle, e.g. Elco Series 8290 IDC socket

Table 8. *Pin assignment of binary I/O lines (X5) on the 40-pin connector*

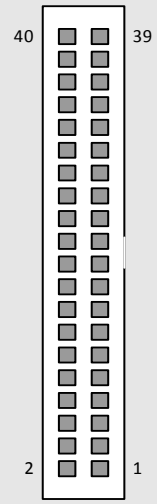
	40 .. 32		39 .. 31		Not used
	30 .. 22		29 .. 21		X3 UART
	20 .. 12		19 .. 11		X4 UART
	10 8 6 4 2	- - - BINSDOUT VCC +5V	9 7 5 3 1	- BINSCS BINSCLK BINSDIN GND	X5 binary I/O

Table 9. *Signal mnemonics of binary I/O interface (X5)*

Signal	Direction	Function
BINSCLK	out	Data clock (SPI interface)
BINSCS	out	Sync signal for the SPI data interface
BINSDIN	in	Serial data for binary inputs (SPI interface)
BINSDOUT	out	Serial data for binary outputs (SPI interface)
GND	-	Digital ground
VCC +5V	out	Power supply +5V DC

2.4 Front-Panel LEDs

The F215 has four status LEDs at the front panel. Three of them are controlled through the onboard FPGA (MEN standard 16Z034_GPIO controller). These lines are user LEDs driven by GPIO lines 0, 1 and 2. Programming these signals as outputs and driving them to logic 0 means the LED is turned on.

You can control the GPIO lines for the three user LEDs using MDIS5 driver software available on MEN's website.

The green *FPGA configured* LED lights up as soon as the FPGA is loaded, i.e. when the UART interfaces are ready for operation.

Table 10. *Front-panel LEDs*

	LED No. / Color	Function
	1 - red	User LED, controlled through GPIO0
	2 - yellow	User LED, controlled through GPIO1
	3 - yellow	User LED, controlled through GPIO2
	4 - green	FPGA configured, lights up when the FPGA is loaded, **not** GPIO-controlled

2.5 CompactPCI Interface

The F215 supports a 32-bit 33-MHz CompactPCI interface fully compatible with CompactPCI specification PICMG 2.0 Rev. 3.0. The board works with 3.3 V VI/O.

For full CompactPCI functionality only the J1 connector is needed, therefore the board only has a J1 connector to the bus.

Connector type of J1:

- 110-pin shielded, 2mm-pitch, 5-row receptacle according to IEC 917 and IEC 1076-4-101

The pin assignment of connector J1 as defined in the CompactPCI specification will not be repeated here.

3 FPGA

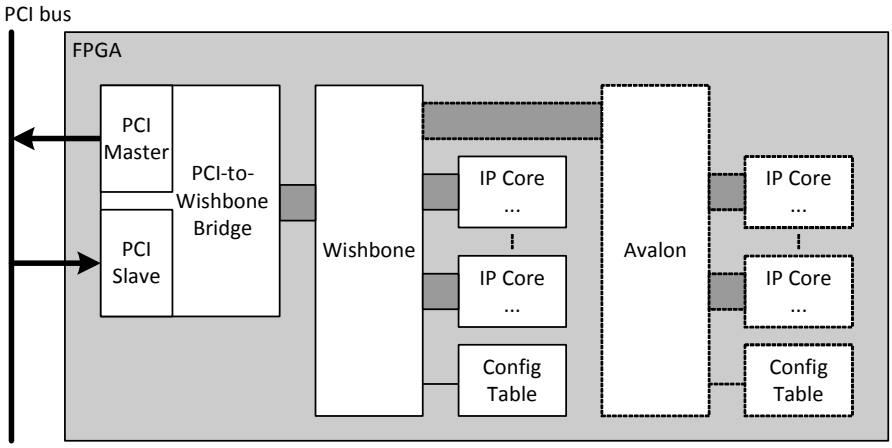
3.1 General

The FPGA – as a part of the F215 – represents an interface between a user-selectable configuration of I/O modules (IP cores) and the PCI bus. The PCI core included in the FPGA is a PCI target. It can be accessed via memory single/burst read/write cycles.

The Wishbone bus is the uniform interface to the PCI bus. However, the FPGA may have multiple internal buses, so that IP cores can be connected to one of several internal buses, e.g., Wishbone or Avalon. This guarantees the highest possible flexibility for different configurations of the FPGA.

Typically each implementation contains basic system functions such as reset and interrupt control etc. and the system library, which are also IP cores.

Figure 7. *FPGA – Block diagram (exemplary)*



A configuration table provides the information which modules are implemented in the current configuration. Furthermore the revision, the instance number (one module can be instantiated more than one time), the interrupt routing and the base address of the module are stored. At initialization time, the CPU has to read the configuration table to get the information of the base addresses of the included modules.

Note that with regard to the FPGA resources such as available logic elements or pins it is not possible to grant all possible combinations of the FPGA IP cores. The following chapter describes one possible configuration of the FPGA. Please ask our sales staff for other configurations.

You can find an overview and descriptions of all available FPGA IP cores on MEN's website.

3.2 Standard Factory FPGA Configuration

The factory FPGA configuration for standard boards comprises the following FPGA IP cores:

- 16Z024-01_Chameleon – Chameleon table
- 16Z014_PCI – PCI-to-Wishbone Bridge
- 16Z100_WBBUS – Wishbone Bus Interconnection Unit
- 16Z069_RST – Reset controller
- 16Z052_GIRQ – Interrupt controller
- 16Z126_SERFLASH – Serial Flash controller
- 16Z029_CAN – CAN controller (controls CAN X1)
- 16Z029_CAN – CAN controller (controls CAN X2)
- 16Z125_UART – UART controller (controls UARTs X3/X4)
- 16Z037_GPIO – GPIO controller with serial interface (8 I/O lines on X5)
- 16Z034_GPIO – GPIO controller (3 outputs for LEDs)

4 Appendix

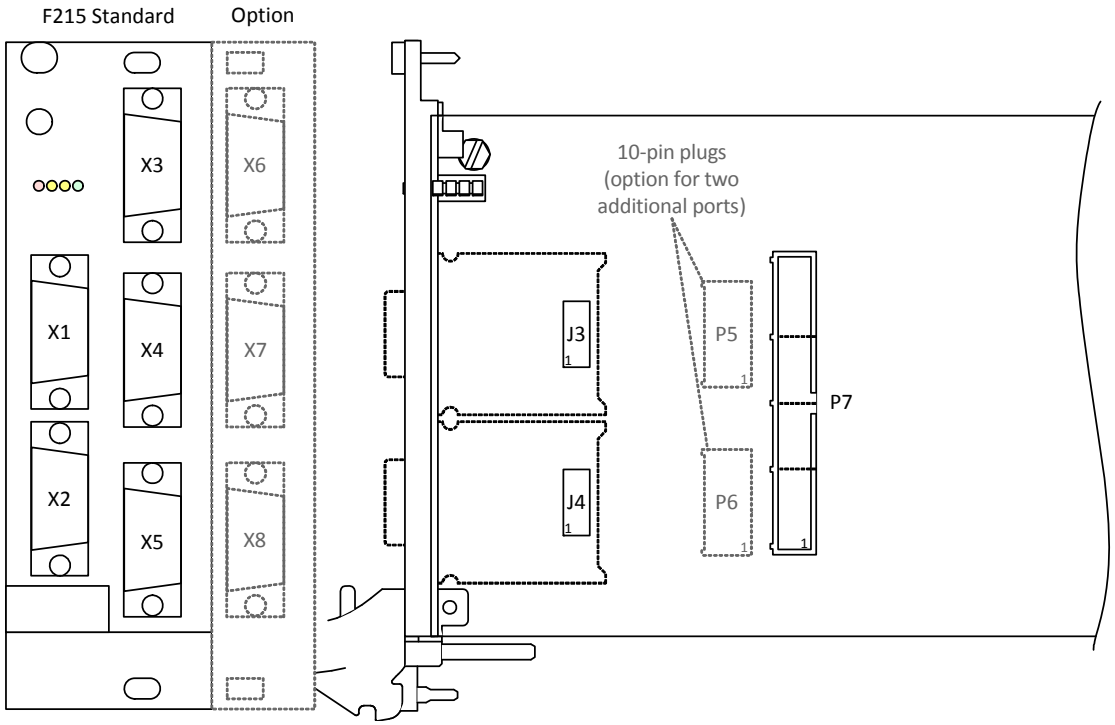
4.1 Assignment of Onboard Connectors to Front-Panel Slots

The interface designation by "Xn" is a generic numbering to facilitate allocation of the interfaces on the front panel. The following table and figure give an example assignment that includes the connector designations, based on the standard version of the board.

Table 11. *Assignment of onboard connectors to front-panel slots*

Onboard Connector	Front-Panel Slot	Standard Function
J3	X1	CAN bus
J4	X2	CAN bus
P5	X7	Not used
P6	X8	Not used
P7, pins 1..10	X5	Binary I/O
P7, pins 11..20	X4	UART
P7, pins 21..30	X3	UART
P7, pins 31..40	X6	Not used

Figure 8. *Assignment of onboard connectors to front-panel slots*



4.2 PCI Configuration

The F215 has the following IDs on the PCI bus:

- PCI Device ID: 0x4D45
- PCI Vendor ID: 0x1A88
- Subsystem Device ID: 0x5A14
- Subsystem Vendor ID: 0x006A

4.3 Literature and Web Resources

- F215 data sheet with up-to-date information and documentation:
  www.men.de/products/02F215-.html
- MEN SA-Adapters:
  www.men.de/products/search,SA--Adapters,accessories.1.html

4.3.1 CAN Bus

- CAN in Automation e. V.
  www.can-cia.de

4.3.2 CompactPCI

- CompactPCI Specification PICMG 2.0 R3.0:
  1999; PCI Industrial Computers Manufacturers Group (PICMG)
  www.picmg.org
- PCI Local Bus Specification Revision 2.2:
  1995; PCI Special Interest Group
  P.O. Box 14070
  Portland, OR 97214, USA
  www.pcisig.com

4.4 Finding out the Board's Article Number, Revision and Serial Number

MEN user documentation may describe several different models and/or hardware revisions of the F215. You can find information on the article number, the board revision and the serial number on two labels attached to the board.

- **Article number:** Gives the board's family and model. This is also MEN's ordering number. To be complete it must have 9 characters.
- **Revision number:** Gives the hardware revision of the board.
- **Serial number:** Unique identification assigned during production.

If you need support, you should communicate these numbers to MEN.

Figure 9. *Labels giving the board's article number, revision and serial number*